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Title: JP2001044269A2: MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT
Country: JP Japan
Kind: A2 Document Laid open to Public inspection
Inventor: KITAMURA WAHEI;
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Application Number: JP19932000181320
IPC Code: H01L 21/68; G01R 31/26;
Priority Number: 2000-01-01 JP20002000181320
Abstract:



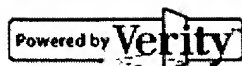
PROBLEM TO BE SOLVED: To surely prevent shift of leads and deformation of the leads by visual inspection of a semiconductor integrated circuit device, in a tray for housing the device.

SOLUTION: A pocket 3 for housing a semiconductor integrated circuit unit 2 is provided in the side of the surface 1a of a tray 1 for housing and tweezers holes 4, for taking out the unit 2 from the pocket 3 by tweezers or the like are formed in the surface 1a by a molding integral with the pocket 3 in each side of the four sides of the pocket 3. These holes 4 are formed by projecting protrusions from the side of the surface 1a of the tray 1 toward the side of the rear of the tray 1, and the unit 2 on the surface of the tray 1 is suppressed of its movement by these protrusions.

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Family: None

Other Abstract Info: DERABS G2001-250502 DERABS G2001-250502



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